A Wide Input Range Dual Path CMOS Rectifier for RF Energy Harvesting

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***Abstract*—**This paper bestows a dual-path CMOS rectifier with adaptive control for Ultra-High Frequency (UHF) RF energy harvesters. The input power range with high power assemblage efficiency (high-PCE) of the rectifier is extended by the proposed architecture which includes a low power path and a high-power path. The dual path rectifier with an adaptive control circuit is fabricated in a 65 nm CMOS process. In proposed order using two inverters for micrify the power consumption at output. Operating at 900 MHz and driving a 147 kΩ load resistor, the measured PCE of this work can be conserve above 20% with an 11 dB input range from −16 dBm to −5 dBm, while only an 8 dB input range can be achieved with long established single path rectifiers. A susceptibility of −17.7 dBm is measured with 1 V output voltage across a capacitive load.

***Keywords*—**Adaptive Control Circuit; CMOS Rectifier; Dual Path Rectifier; Energy Harvesting; Power Convention Efficiency.

***Abbreviations*—**Integrated Circuit (IC); Power Conversion Efficiency (PCE); Very-Large-Scale Integration (VLSI); Ultra-High Frequency (UHF).

I. INTRODUCTION

VERY-Large-Scale Integration (VLSI) is the bout of fabricating an Integrated Circuit (IC) by blending thousands of transistors into a single chip. VLSI initiated in the 1970s when involute semiconductor and communication technologies were being progressed. The microprocessor is a VLSI device. Before the initiation of VLSI technology, most ICs had a obligatory set of functions they could execute. An electronic circuit valor consist of a CPU, ROM, RAM and other mastic logic. VLSI lets IC inventors add all of these into one chip. The electronics productiveness has achieved a uncommon growth over the last few decades, mainly due to the quick advances in large scale integration technologies and system design applications. With the arrival of VLSI designs, the number of applications of ICs in high-performance reckon, controls, telecommunications, image and video processing, and consumer electronics has been rising at a very fast rate. The current cutting-edge technologies such as high persistence and low bit-rate video and cellular communications confer the end-users a spectacular amount of applications, processing power and portability. This alleviate is expected to grow rapidly, with very important hint on VLSI design and systems design.

The embody of VLSI was molded more than thirty years ago to describe the process of formulating, cunning and fabricating integrated circuits by combining thousands of transistors and their interconnections in a single chip. This transpired when the available MOS technologies had a feature size larger than 1 µm. As technology evolved toward smaller sizes, decreasing more and more, the term VLSI was applied to chips formed by hundreds of thousands and even hundreds of millions of transistors. Since then, the minimum dimensions have been diminishing down even more as we handle today billions of transistors.

II. RELATED WORKS

In order to improve the susceptibility, the antenna-rectifier interface is examined as it plays a resolvable role in the co-design optimization. eventually, a 5-stage cross-connected differential rectifier with a 7-bit binary-weighted capacitor bank is designed and fabricated in standard 90 nm CMOS technology. The rectifier is escort at resonance with a high-Q loop antenna by means of a control loop that remunerates for any variation at the antenna-rectifier interface and passively promotes the antenna voltage to augment the sensitivity. A complementary MOS diode is proposed to improve the harvester's power to store and hold energy over a long period

of time during which there is scanty power for rectification [Mark Stoopman et al., 1]. A high-efficiency CMOS rectifier circuit for UHF RFIDs was flourished. The rectifier has a cross-coupled bridge configuration and is driven by a differential RF input. A differential-drive active gate bias mechanism concurrently enables both low ON-resistance and small reverse leakage of diode-connected MOS transistors, resulting in large Power Conversion Efficiency (PCE), especially under small RF input power conditions [Hameed & Moez, 2]. While the functionality of emerging wireless microsensors, cellular phones, and biomedical grafts, to name a few, is on the rise, their dimensions continue to retrace. This is wretched because smaller batteries fatigue quicker. Not surprisingly, recharging batteries wirelessly is deserved progressively popular today. Still, small pickup loops cannot tackle much, so induced EMF voltages $v_{EMF.S}$ are low. Modern receivers can resonate these low input voltages to rectifiable proportions, but only with a finely tuned capacitor that resonates at megahertz when on-chip and at kilohertz when off-chip [Hiroyuki Nakamoto et al., 3]. Charge balance law based on aegis of charge is stated and enrolled to analyze on-chip linear, Fibonacci and exponential charge pumps. For micro-power on-chip executions, both the positive and the negative-plate parasitic capacitors have to be considered. Voltage conversion ratios and proficiencies can be obtained in closed form for single- and dual-branch linear charge pumps, but not for Fibonacci and exponential charge pumps [Kotani et al., 4]. Rectifiers are pertinent energy converters and hereafter resolvable building blocks for RFID applications. In the first half of the work, we have granted a design methodology for analogous the rectifier input impedance with the antenna to maximize the rectifier power conversion efficiency [Lazaro & Rincon-Mora, 5]. Multiple energy sources, such as sunlight, vibration, thermal and RF energy, are potential candidates for various energy harvesting applications. While some sources are limited by the application scenarios, the density of wireless devices keep increasing rapidly extensive in this decade. And most of the communication systems operate in the ultra-high frequency (UHF, 300 MHz to 3GHz) ISM bands. However, a high leakage current will occur at high input amplitude conditions because the PMOS and NMOS will be turned-on simultaneously during the transition period, which is a similar problem to the tendire-through current of a CMOS inverter.

III. Power Convention Efficiency

As dispute overhead, the single-path CC topology can only reform the PCE for a confined limited operation range. To inquire the staging of the CC rectifier, the imitation PCEs confronting the input power PIN with 6 types of transistors procurable in a 65 nm CMOS process with the same transistor sizes. The 6 types of transistors include the low threshold (LVT), standard threshold (SVT), and high threshold (HVT) of the general-purpose (GP) transistors and also the congruent low-power (LP) version transistors. Meantime, the broadness of the PMOS are set to be 2 times of that of the NMOS, and all the channel lengths are the minimum. The simulation effects show that the peak PCE could be executed at different PIN by selecting a precise type of transistor and an ideal size. For example, the maximum PCEs achieved at PIN = −8 dBm and RL = 100 kΩ m or LVTLPμwith NMOS LVTGP transistors having W = 2.5 m are 62% and 46%, respectively.μ transistors with W = 150 Almost, low VTH transistors can achieve better PCE at lower PIN, and high VTH transistors can achieve a higher peak PCE. Figure 4 shows the basic conceptual idea used in this work [Véronique Kuhn et al., 6; Facen & Boni, 7].

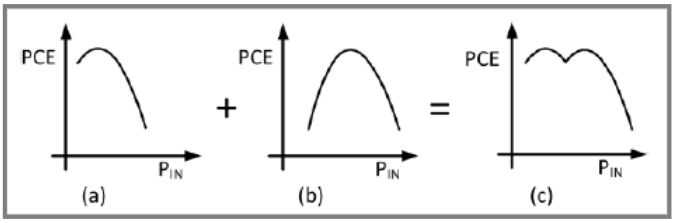

Figure 1: Efficiencies of the Conventional Rectifier
(a) Optimized at Low Power, (b) Optimized at High Power, and (c) The PCE of the Proposed Dual-Path Rectifier

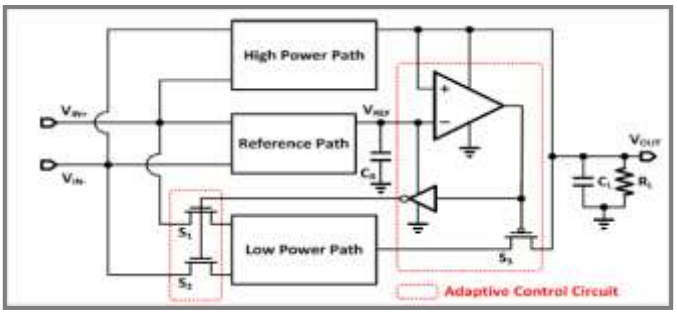

Figure 2: System Architecture of the Dual-Path Rectifier

The block diagram of the advanced rectifier is shown in Figure above. The dual-path rectifier consists of a low power path using LVTGP transistors for high-PCE at low input power and also for superior input delicacy, a high power path using LVTLP transistors designed for high-PCE at high input power, a reference path that generates a threshold voltage for the electronic path selection, and 3 switches S1 through S3 to enable/disable the low power path. Thus, the system can automatically choose the pertinent path according to the input power level to achieve a wider high-PCE range. And of course, the thick-oxide IO devices can also be a choice for the high-power path. One problem is that, the input impedance of the rectifier with IO devices would vary more from that of the rectifiers all using the thin-oxide devices. This makes the matching network more difficult to satisfy the two paths unaccompanied additional tuning control [Wing-Hung Ki et al., 8; Haojuan Dai et al., 9].

The reference path is also a CC rectifier path using the parallel type of transistors and the same figure of stages as the high power path. But it only extensions the input of the comparator and an inverter. Then, it can bestow a relatively high voltage, when comparing with the high power path which drives a resistive load. The comparator with built-in offset contrast the VREF and VOUT to select the path [Yi et al., 10].

IV. RESULT

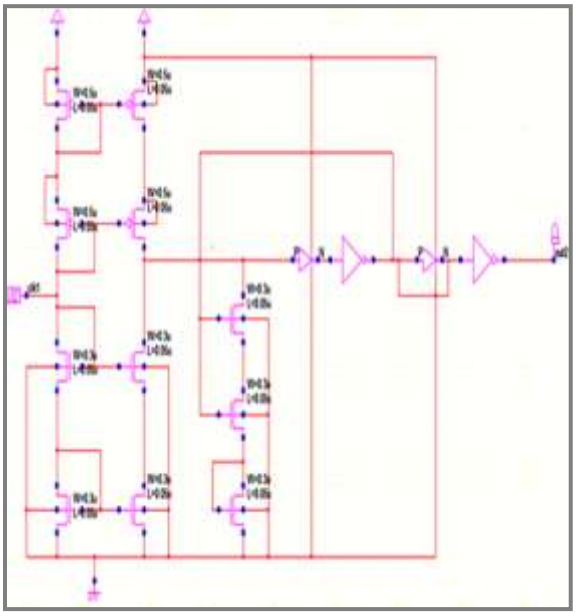

Figure 3: LAYOUT-Dsch

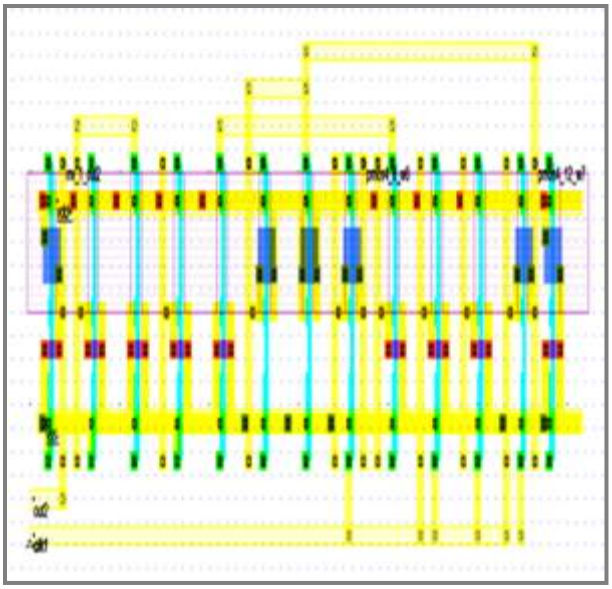

Figure 4: LAYOUT-MICROWIND

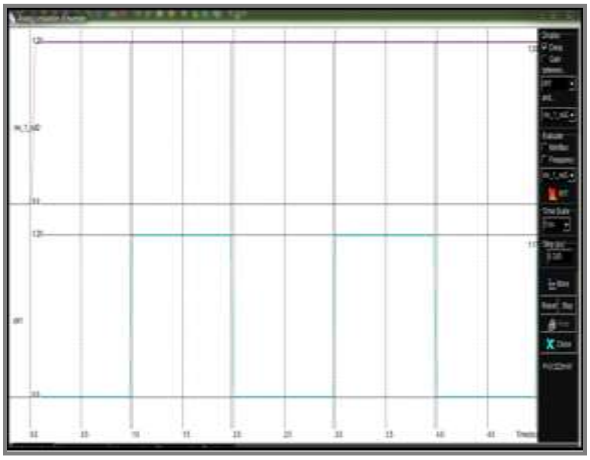

Figure 5: Voltage and Current

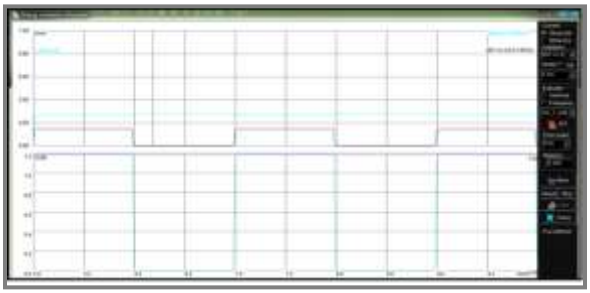

Figure 6: Voltage Vs Voltage

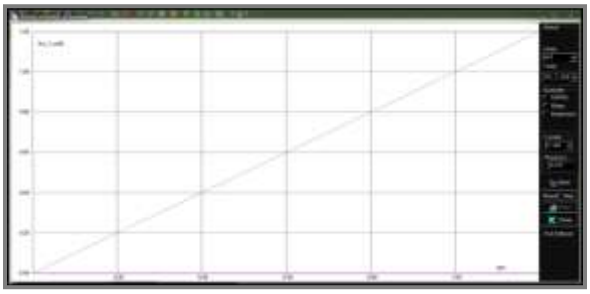

Figure 7: Voltage Vs Time

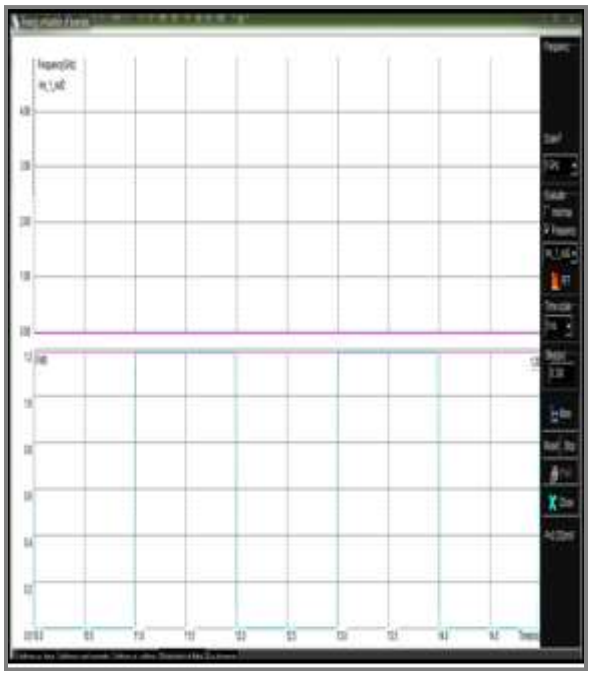

Figure 8: Frequency Vs Time

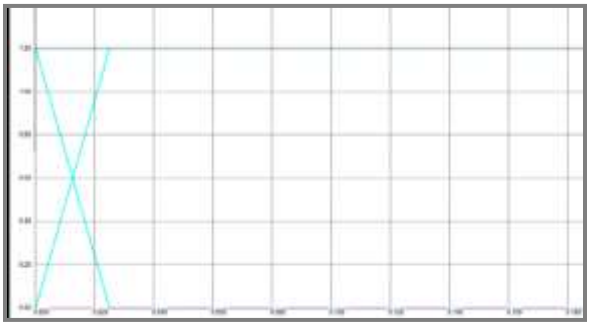

Figure 9: Eye Diagram

V. CONCLUSION

This paper bestows a UHF RF energy harvester that features an capable dual-path structure with adaptive auto-select control that sustains high PCE for a wide range. A common-gate input comparator with hysteresis is offered to switch the path with little power raised. Implemented in a 65 nm CMOS technology, a sensitivity of −17.7 dBm for 1 V output with a capacitive load is measured. The above 20% PCE range of the offered RF energy harvester can be maintained from −16 dBm to −7 dBm with a range of 11 dB, while the single-path rectifiers can only maintain the high-PCE range for an 8dB range.

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